REMARKS

Claims 1 through 51 are pending in the application. Allowance of claims 1 through 15 is appreciated. Claims 16, 20, 24, 26, 31 and 32 are amended while independent claims 31 through 51 are added.

Rejection of Claims 1-34 under 35 U.S.C. § 251

The Examiner objected to the reissue Declaration, and rejected claims 1-34 as based upon a defective reissue Declaration, under 35 U.S.C. § 251. The Examiner objected to the Declaration filed with this application "because none of the errors which are relied upon to support the reissue application are errors upon which a reissue can be based", and that "the oath does not specifically mention an error correctable by reissue for the new claims 16-34." Applicant respectfully traverses the Examiner's rejection for the following reasons.

The Examiner asserts that the reissued Declaration "does not specifically mention an error correctable by reissue for the new claims 16-34." The Examiner asserts that "Merely stating [that] the claims are broader is not enough." Applicant tends to disagree because, under the current revision of 37 C.F.R. § 1.157(a)(1), the reissue Declaration is required to state little more than "at least one error being relied upon as the basis for reissue." This the reissue Declarations have done, as is explained below.

It is important to note that Applicant's reissue Declaration, on page 2, expressly defined one error in claim 7. Moreover, there is no longer any onerous requirement set forth in 37 C.F.R. §1.175 to identify "an error correctable by reissue of each of the new claims 16-23", because rule §1.157(a)(1) simply requires the statement of "at least one error being relied upon as a basis for

reissue."

The Examiner kindly suggested that the reissue Declaration be amended to state that phrases such as "skipping a remaining data address mark" as defined by claim 1 or "detecting said address mark" as defined by claim 7, were not required for patentability. In response with the Examiner's suggestion, and in conformance with the requirement set forth in 37 C.F.R. §1.175(b)(1)(ii), Applicant submits herewith a Supplemental Declaration signed by the Assignee and the inventor, to comply with the Examiner's requirement. Accordingly, this rejection of claims 1-34 as based upon a defective reissue Declaration under 35 U.S.C. § 251, is rendered moot. Withdrawal of the rejection is therefore requested.

The Reissue Declaration

In paragraph 4 on Page 2 of the Examiner's comments, the Examiner stated that the "original patent, or statement as to the loss or inaccessibility of the original patent, must be received before reissue application can be allowed. See 37 CFR §1.178." The Examiner's attention is invited to the fact that the original Declaration by the Assignee expressly declared that:

> "I offer to surrender the original grant of the patent, but the patent is lost or has become unavailable."

The substitute Declaration by the Assignee now expressly states that "I offer to surrender the original grant of the patent, but that patent has become lost and has become inaccessible.", in conformance with the express language of 37 C.F.R. § 1.178(a). The executed Substitute Declarations by the Assignee and by the Inventor will be submitted as soon as Applicant's

undersigned attorney receives such executed Declarations. Accordingly, withdrawal of the objection is respectfully requested.

Allowable Subject Matter

In paragraph 12 of the Office action, the Examiner objected to claims 18, 19, 22, 23, 25, 27, 29, 30, 33 and 34 for dependency upon a rejected base claim, and stated that these claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Rejection of Claims 16, 20, 24, 26 and 31 under 35 U.S.C. § 102(e) by anticipated by Suzuki '582

In paragraph 6 of the Office action, the Examiner rejected claims 16, 20, 24, 26 and 31 under 35 U.S.C. §102(e) for alleged anticipation by Suzuki U.S. Patent No. 5,742,582. Applicant respectfully traverses this rejection for the following reasons.

Suzuki '582 shows a data regions split into two different data blocks, with each data block containing only **one** data address mark (*see* Fig. 4 of Suzuki '582, where each of the data blocks "DATAa" and "DATAb" have only one data address mark). According to the system shown in Suzuki '582, when that one data address mark associated with the data block, "DATAa," is defective, the data block cannot be accessed. Similarly, the data block, "DATAb," cannot be accessed when the one data address marks associated thereto is defective. In essence, Suzuki '582 is similar to and suffers from all of the disadvantages associated with Applicant's Fig. 1 discussed in Applicant's background discussion. *See, e.g.*, column 3, lines 7-14 of the original patent of the instant reissue application. In contradistinction, the pending claims each define a data block that contains two or more DAMs even if that data block is a portion of a split data

region. Suzuki '582 never suggests either any more than a single data address mark associated with each single data block, or any more than a single data address mark associated with each data region of a split data region. *See* Gold '545, at column 7, lines 16-22. In view of these distinctions therefore, the ***all elements*** rule demands withdrawal of this anticipation rejection.

Rejection of Claims 20, 26 and 31 under 35 U.S.C. § 102(e) as anticipated by Gold '542

In paragraph 7 of the Office action, the Examiner rejected claims 20, 26 and 31 under 35 U.S.C. §102 for alleged anticipation by Gold U.S. Patent No. 5,231,545. For the reasons stated below, Applicant respectfully traverses this rejection.

In support of this rejection, the Examine asserts that Gold '545 "teaches recording at least two data address marks in a plurality of different locations along a data track." The Examiner's comments, page 2. This is incorrect because Gold '545 shows one ID AM and one DAM (with an address mark type field 18 distinguishing between the ID header 22 and the data header 24) (See Gold '545 at column 8, lines 66, 67), while Applicant's rejected claims define two DAMs in a data block. Absent anticipation of ***all elements*** of the pending claims by Gold '545, this rejection must be withdrawn and claims 20, 26 and 31 allowed over Gold '545.

Rejection of Claims 17, 21, 28 and 32 under 35 U.S.C. § 103 (a) over Suzuki '582 and Gold '545

In paragraph 9 of the Office action, the Examiner rejected claims 17, 21, 28 and 32 under 35 U.S.C. §103(a) as rendered obvious, and unpatentable over the Examiner's proposed combination of Suzuki '582 modified in view of Gold '545. For the reasons stated below, Applicant respectfully traverses this rejection for the following reasons.

In support of this rejection the Examiner argues that,

> "It would have been obvious to one of ordinary skill in the art to utilize that teaching of Gold ('545) to provide *first* and *second* data address marks comprising a plurality of bits and different patterns ... ."

The fallacy in the Examiner's argument is that the Examiner's interpretation of Gold '545 is not only wholly absent from Gold '545, but is contrary to the express teachings of Gold '545. As clearly shown in Figure 1A cited by the Examiner, and clearly illustrated in Figure 2, as well as in column 8, lines 61 through 65, Gold '545 nowhere discloses a first data address mark and a second data address mark in a specific data block as required by dependent claim 17, and consequently never teaches two data address marks in any data block. The *data blocks* 20 in Gold '545 are clearly labeled in Figure 1A. As illustrated by Figures 1A and 2, each data block contains one ID AM (that is, an ID address mark) and one DAM (that is, one data address mark); there is no disclosure of two *DAM's* in any data block in Gold '545. Consequently, Gold '545 suffers from all of the deficiencies noted in Applicant's background discussion. Moreover, the fact that Applicant alone both recognizes those deficiencies and remedy those deficiencies by providing both first and second data address marks in each data block, serves independently as additional and convincing indicia non-obviousness. Withdrawal of the rejection under 35 U.S.C. §103(a) is therefore required.

Rejection of Claims 21, 28 & 32 Under 35 U.S.C. §103(a) Over Suzuki '582 and Gold '545

Claims 21 28 and 32 were separately rejected under 35 U.S.C. §103(a) as rendered obvious, and unpatentable, over the Examiner's proposed combination of Suzuki '582 modified

according to Gold '545. Applicant respectfully traverses this rejection for the following reasons.

In support of the rejection, the Examiner again asserts that:

> "It would have been obvious to one of ordinary skill in the art to utilize the teaching of Gold ('545) to provide *first* and *second* data address marks comprising a plurality of bits and different patterns, motivation being to provide fault tolerant decoding as set forth in col. 1 (,) lines 5-12 of Gold ('545)."

As earlier explained, Gold teaches only a *single* address mark in each data block. In Figures 1A and 2 illustrating the contents of each data block, Gold discloses a data address mark following an ID address mark (see rows A and B) in Fig. 2. As explained in column 8, lines 26 and 27 of Gold '545,

> "(t)he first and second pattern fields 14 and 16 **together** provide **the** address mark pattern."

As explained by Gold '545, the Examiner's proposed combination has two address marks, the first being the ID address mark and the second being a data address mark, a scheme where:

> "The desired address mark pattern essentially comprises a first 7 zero pattern, immediately followed by a second 7 zero pattern." Gold '545 at column 8, lines 29-30.

Gold uses consecutive seven zero patterns for both the data address mark and the ID address mark, as illustrated in rows A and B in Figure 2; this does not endow the Examiner's proposed combination with Applicant's "*first* and *second* data address marks" as defined by the pending claims. Absent these features, as well as the failure of the Examiner's proposed combination to either recognize or remedy such deficiencies in the art has the inability to read the data block upon encountering the failure to read the several data address mark that Applicant both recognizes and remedies by redundant data address marks, is further and persuasive evidence of

non-obviousness. Consequently, withdrawal of the rejection is required.

Amendments Under 37 C.F.R. §1.173(c)

Independent claims 16, 20, 24, 26, 31 and 32 have been amended. These amendments add the phrase "preceding a servo information area" in a preamble, and define the location of either one, or both of the data address marks relative to the servo information area. Support in the disclosure of the patent for these changes is found beginning in line 59 of column 5 and continuing through line 19 at column 6. Additionally, Figure 6 shows the detailed format of one of Applicant's two data marks in the data field which is illustrated in Figure 3, as a component of an exemplary data arcuate sector by Figure 1.

Newly Presented Claims 35-51 under 35 C.F.R. § 1.173(c)

As discussed during the Office interview, Applicant has presented as newly added claims 35 through 51, alternative definitions of Applicant's inventions as defined by independent claims 16, 20, 24, 26, 31 and 32. The language of claims 35 through 37 is based upon independent claim 16, while the language of claims 38 through 40 is based upon independent claim 20. The language of independent claims 41 through 43 is based upon independent claim 24 while the language of independent claims 44 through 46 is based upon independent claim 26. The language of independent claims 47 through 49 is based upon independent claim 31 while the language of independent claims 50 and 51 is based upon independent claim 32. These features of claims 35, 38, 41, 44, 47 and 50, including the second data address mark "that is distinguishable from said first data address mark" are supported by the specification beginning on line 59 of

column 5 and continuing through line 19 of column 6, and illustrated in Fig. 6 with two data marks in the data field illustrated by Fig. 3. Additionally, column 5, lines 65 and 66 define Applicant's "two data address marks [as being] respectively distinguished ... ."

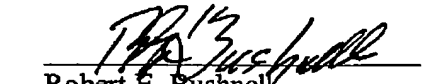
The feature of the second address mark "exhibiting a different bit pattern" as defined by independent claims 36, 39, 42, 45 and 48 is also supported by the specification beginning on line 59 of column 5 and continuing through line 19 in column 6, and is illustrated by Fig. 6. Moreover, column 5, lines 65 and 66 explain that Applicant's "two data address marks are respectively distinguished by using different patterns ... ."

Applicant's reading and writing of two data address marks as defined in independent claims 37, 40, 43, 46, 49 and 51 with the marks "separately marking said data block" is defined in columns 5 and 6, illustrated by Fig. 6, explained in column 5, lines 65-67 with the two data address marks [being] respectively distinguished by using different patterns, and [being] discriminated by the microcomputer 14." Additionally, column 6, lines 1-9 explain that "when only one byte of data address mark is detected among two bytes of data address marks, it is regarded as an effective data address mark." This explanation is continued through lines 10-39.

In view of the above, all claims are deemed to be allowable and this application is believed to be in condition to be passed to issue. Reconsideration of the rejections and objections is requested. Should any questions remain unresolved, the Examiner is requested to telephone Applicant's attorney.

A fee of $1,734.00 is incurred by the addition of seventeen (17) independent claims in excess of nine (9), and seventeen (17) total claims in excess of total thirty-four (34). The Commissioner is authorized to charge Deposit Account No. 02-4943 of Applicant's undersigned attorney in the amount of such fees.

Respectfully submitted,



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MARKED-UP VERSION OF AMENDMENTS

IN THE CLAIMS

Please amend claims 16, 20, 24, 26, 31 and 32 as follows, and add new claims 35 through 51, as set forth above.

16. (Amended) A method of providing a data block **preceding a servo information area** in a magnetic recording medium for accessing user data therefrom, comprising:

writing a first data address mark in said data block; and

writing a second data address mark in said data block **at a location preceding said servo information area**.

20. (Amended) A magnetic recording medium having a data track having one or more data blocks **preceding a servo information area**, comprising:

a first data address mark **located before said servo information area in a first data block**; and

a second data address mark **located before said servo information area in said first data block**.

24. (Amended) A disk drive device**, comprising:**

[having] a magnetic recording medium having at least one data block that includes at least a first data address mark and a second data address mark[, comprising:] **having no servo**

information area therebetween; and

a controller configured to read within said at least one data block at least one of said first data address mark and said second data address mark[, and if said first data address mark is read successfully, synchronizing said data block with a user data access according to said first data address mark, said controller synchronizing said data block with said user data access according to said second data address mark if said second data address mark is read successfully].

26.(Amended) A method for reading a data [track] **block preceding a servo information area** of a memory disk, said method comprising the steps of[:

recording at least two] **reading at least one of a plurality of** data address marks [on the memory disk in a plurality of different recording locations along said data track] **recorded on said data block at a location before said servo information area**[;

establishing synchronization by detecting a select one of said at least two data address marks from one of said plurality of different recording locations; and

characterizing the detected said data address mark as an effective data address mark of said corresponding data region on said data track].

31.(Amended) A method for preparing a memory disk, comprising:

recording a data address mark providing synchronization that enables reading of data from the memory disk, [at a first location] along a data track on the memory disk at a first location **on a first data block** preceding a [corresponding data track] **servo information area**;

and

recording said data address mark at a second location **on said first data block** preceding said [corresponding data track] **servo information area.**

32.(Amended) A disk drive device, comprising:

a head positioned to read, within [each] **at least one of a plurality of** data [block] **blocks** of a recording medium, a first data address mark [exhibiting a first bit pattern], and a second data address mark, **said first data address mark and said second data address mark having no servo information therebetween** [exhibiting a second and different bit pattern]; and

a controller regulating movement of said head [and discriminating between said first bit pattern and said second bit pattern] **based on at least one of said first data address mark and said second data address mark.**